In the Claims

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Previously presented) A mechanism for preventing ESD damage to a electronic device comprising at least one connection area having a plurality of pads (P_1 to P_n) arranged sequentially for mounting to an integrated circuit, and a plurality of fan-out signal lines (F_1 to F_n) extending from the pads (P_1 to P_n) respectively, the pads P_1 and P_n disposed on outermost sides of the connection area, the mechanism comprising:

a plurality of ESD protection device (ES_1 to ES_n) configured corresponding to the fan-out signal lines (F_1 to F_n);

wherein, impedances of the ESD protection devices ES_1 and ES_n are smaller than impedances of the other ESD protection devices ES_2 to ES_{n-1}.

2. (Original) The mechanism as claimed in claim 1, wherein each ESD protection device comprises at least one element having a MOS transistor circuit structure and equivalent channel widths of the ESD protection devices ES_1 and ES_n are longer than equivalent channel widths of the other ESD protection devices ES_2 to ES_{n-1}.

3. (Previously presented) A mechanism for preventing ESD damage to a electronic device comprising at least one connection area having a plurality of pads (P_1 to P_n) arranged sequentially for mounting to an integrated circuit, and a plurality of fan-out signal lines (F_1 to F_n) extending from the pads (P_1 to P_n) respectively, the pads P_1 and P_n disposed on outermost sides of the connection area, the mechanism comprising:

a plurality of ESD protection device (ES_1 to ES_n) configured corresponding to the fan-out signal lines (F_1 to F_n);

wherein, impedances of the ESD protection devices ES_1 to ES_j gradually increase and impedances of the ESD protection devices ES_{j+1} to ES_n gradually decrease, $1 < j < n$.

4. (Original) The mechanism as claimed in claim 3, wherein each ESD protection device comprises at least one element having a MOS transistor circuit structure, equivalent channel widths of the ESD protection devices ES_1 to ES_j gradually decrease, and equivalent channel widths of the ESD protection devices ES_{j+1} to ES_n gradually increase.

5. (Previously presented) A mechanism for preventing ESD damage to a electronic device comprising at least one connection area having a plurality of pads (P_1 to P_n) arranged sequentially for mounting to an integrated circuit, and a plurality of fan-out signal lines (F_1 to F_n) extending from the pads (P_1 to P_n) respectively, the pads P_1 and P_n disposed on outermost sides of the connection area, the mechanism comprising:

a plurality of ESD protection device (ES_1 to ES_n) configured corresponding to the fan-out signal lines (F_1 to F_n);

wherein, an impedance of one ESD protection device ES_k is different from impedances of the other ESD protection devices, $1 \leq k \leq n$.

6. (Original) The mechanism as claimed in claim 5, wherein each ESD protection device comprises at least one element having a MOS transistor circuit structure and an equivalent channel width of the ESD protection device ES_k is different from equivalent channel widths of the other ESD protection devices.

7. (Previously presented) A liquid crystal display panel, comprising:

a pixel array;

at least one connection area having a plurality of pads (P_1 to P_n) arranged sequentially for mounting to an integrated circuit, wherein the pads P_1 and P_n are disposed on outermost sides of the connection area;

a plurality of fan-out signal lines (F_1 to F_n) extending from the pads (P_1 to P_n) respectively; and

a plurality of ESD protection devices (ES_1 to ES_n) configured corresponding to the fan-out signal lines (F_1 to F_n);

wherein, impedances of the ESD protection devices ES_1 and ES_n are smaller than impedances of the other ESD protection devices ES_2 to ES_{n-1}.

8. (Original) The liquid crystal display panel as claimed in claim 7, wherein each ESD protection device comprises at least one element having a MOS transistor circuit structure and equivalent channel widths of the ESD protection devices ES_1 and ES_n are longer than equivalent channel widths of the other ESD protection devices ES_2 to ES_{n-1}.

9. (Original) The liquid crystal display panel as claimed in claim 8, wherein the equivalent channel widths of the ESD protection devices ES_1 to ES_j gradually decrease, and the equivalent channel widths of the ESD protection devices ES_{j+1} to ES_n gradually increase, $1 < j < n$.

10. (Previously presented) A liquid crystal display panel, comprising:

a pixel array;

at least one connection area having a plurality of pads (P_1 to P_n) arranged sequentially for mounting to an integrated circuit, wherein the pads P_1 and P_n are disposed on outermost sides of the connection area;

a plurality of fan-out signal lines (F_1 to F_n) extending from the pads (P_1 to P_n) respectively; and

a plurality of ESD protection device (ES_1 to ES_n) configured corresponding to the fan-out signal lines (F_1 to F_n);

wherein, an impedance of one ESD protection device ES_k is different from impedances of the other ESD protection devices, $1 \leq k \leq n$.

11. (Original) The liquid crystal display panel as claimed in claim 10, wherein each ESD protection device comprises at least one element having a MOS transistor circuit structure and an equivalent channel width of the ESD protection device ES_k is different from equivalent channel widths of the other ESD protection devices.

12. (New) The liquid crystal display panel as claimed in claim 10, wherein each ESD protection device comprises at least one element having a MOS transistor circuit

structure and equivalent channel widths of the ESD protection devices ES_1 and ES_n are longer than equivalent channel widths of the other ESD protection devices ES_2 to ES_{n-1}.

13. (New) The liquid crystal display panel as claimed in claim 12, wherein the equivalent channel widths of the ESD protection devices ES_1 to ES_j gradually decrease, and the equivalent channel widths of the ESD protection devices ES_{j+1} to ES_n gradually increase, $1 < j < n$.